Development of a Virtual Test Environment for RF Transceiver Architectures

Background

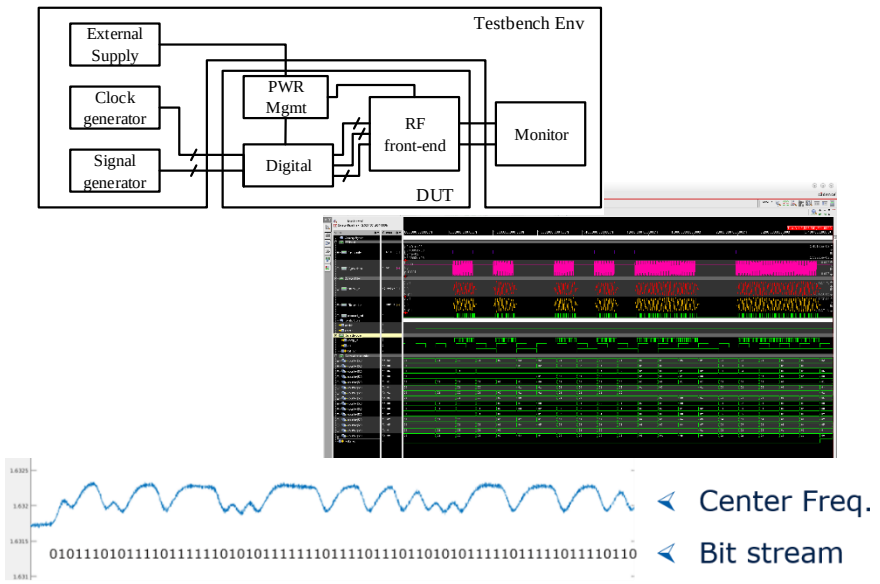
Todays SoCs integrate digital, analog and RF components side by side. Due to the high complexity of such a system an early verification of the system's behavior before producing prototypes is important.

A virtual test environment allows early debugging of the system as well as the planned tests. Reuse of the tests in simulation and on hardware reduces the risk of finding errors later in the process, saving time for actual evaluation of the design.

Task

The thesis aims at developing a virtual testbench for a currently developed transceiver chip at the institute.

After researching common testbench design recommendation and approaches, typical testbench modules should be implemented in the currently used verification environment. This includes different sources and monitoring blocks as well as test evaluation routines. Furthermore the work includes the development of test sequences oriented on the physical tests planned for the chip.



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