Design and Implementation of a Time-to-Digital Converter for All-Digital PLLs in 28nm Technology

Background

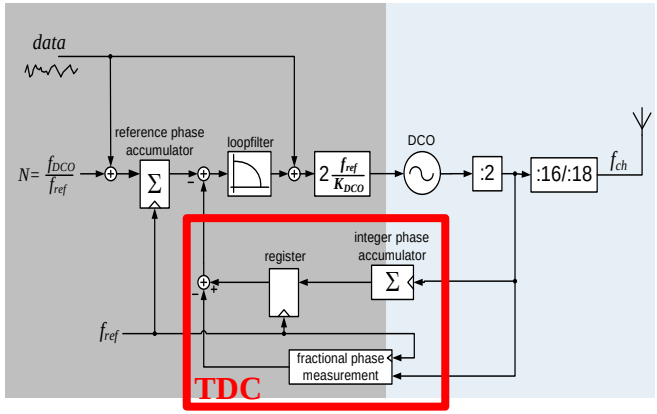
Modern communication standards place high demands on the frequency generation in integrated circuits, especially with regards to low power consumption, low area, low phase noise and spurious tones. All-Digital Phase-Locked-Loops (PLL) in contrast to classical analog PLLs have an advantage in scaling better with advances to smaller CMOS nodes in terms of power and area consumption. But with the high integration density in small nodes power supply noise coupling through substrate or supply becomes a critical factor in such designs.

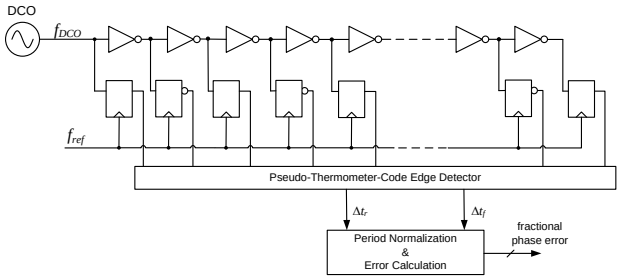
Time-to-Digital converters (TDC) are critical components in the All-Digital PLL design as their resolution and linearity have a direct influence on achievable phase noise and overall performance.

Task

The aim of this thesis is the development of a time-to-digital converter suitable for application in an All-Digital PLL.

Starting from the targeted specification of the PLL, key parameters of the TDC need to be defined. Current architectures should be compare with regards to their possible performance and robustness against disturbances. Afterwards a promising candidate is to be implemented in 28nm and its performance verified in simulation.





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