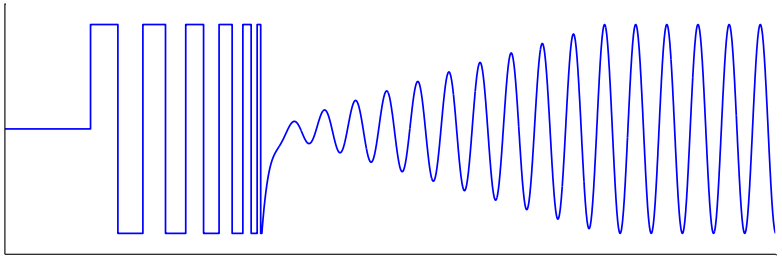
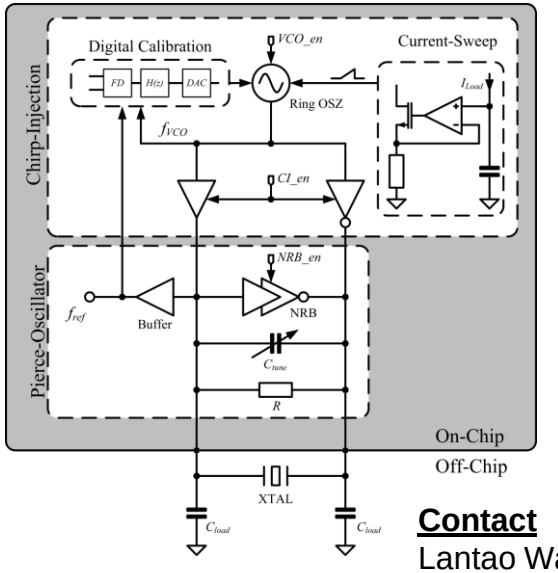
Chair of Integrated Analog Circuits and RF Systems

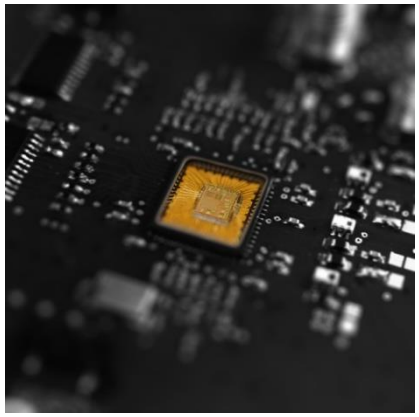
Design of an Integrated Crystal Oscillator in a 28 nm Technology



Background

Phase-locked loop (PLL) serves as the frequency generator, which plays a critical role in wireless communication systems. However, traditional analog PLLs do not scale well with modern advanced technologies due to large area overhead. Therefore, all-digital PLL (ADPLL) has recently received vast attention. An integrated crystal oscillator is a very important component for the ADPLL that is currently under development at IAS, as it will serve as the reference frequency generator. To ensure good performance of the ADPLL, a crystal oscillator with low phase noise is to be implemented.





Task

In this thesis an integrated crystal oscillator is to be implemented in a 28 nm technology. This includes the study of state-of-art architectures, implementation of the circuitry, testbench and performance verification via simulation.

Requirement

- Interested in the topic
- Good knowledge in analog integrated circuit and RF system
- Previous experience with Cadence and Matlab is preferred but not necessary
- Fluent in English

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