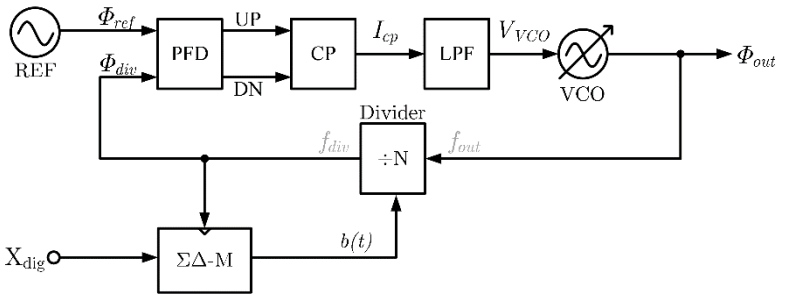
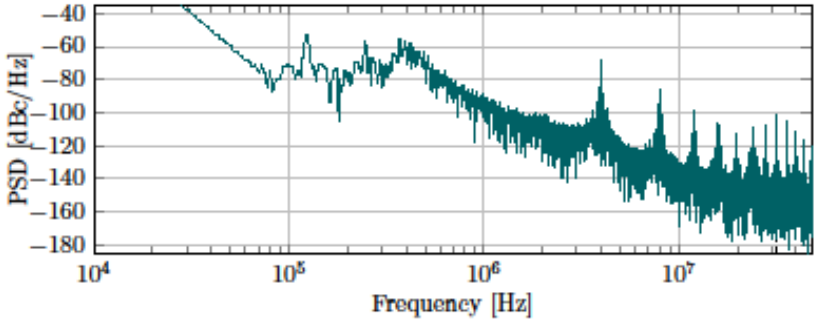
Design and Implementation of an integrated Phase-Locked Loop for Sigma-Delta Analog-to-Digital Converters

Background

Today's wireless communication has become an omnipresent thrive for the most efficient devices being able to handle multiple standards such as Bluetooth, WiFi or Zigbee. As a result complex reconfigurable receiver architectures are required to handle all these different standards at once. The necessary computational effort and signal processing of the data is generally handled by the Digital Signal Processing unit as encountered in every mobile handset.

Any transmitted and received data however, is still analog and thus has to be converted to the digital domain with greatest precision. Most advanced Analog-to-Digital Converter (ADC) rely on ΣΔ Modulator structures to obtain a highly accurate conversion and a more robust operation. Nonethless, some challenges in the design of these ΣΔ-ADCs remain, with clock jitter being on of the prominent issues. By disturbing the sampling instances of the ΣΔ-ADC a severe degradation of the ΣΔ-ADC's performance can occur.





Task

This thesis aims at implementing a Phase-Locked Loop (PLL) which is able to generate a stable, low jitter clock signal for the ΣΔ-ADC of the AixRF chip developed at the chair. Before starting with the design a thorough investigation of the PLL's requirements is necessary. Afterwards a suitable architecture will be chosen and implemented.

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