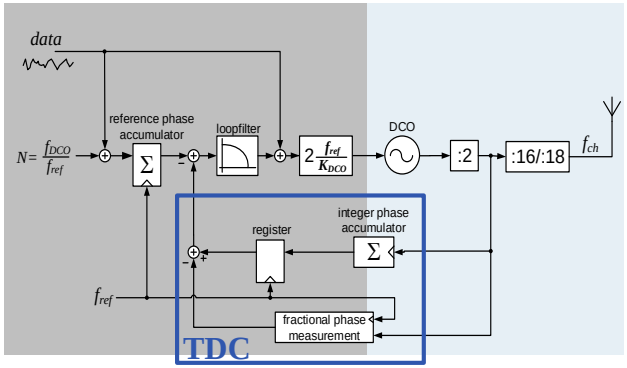
System-level Design and Implementation of an All-Digital PLL in 28nm Technology

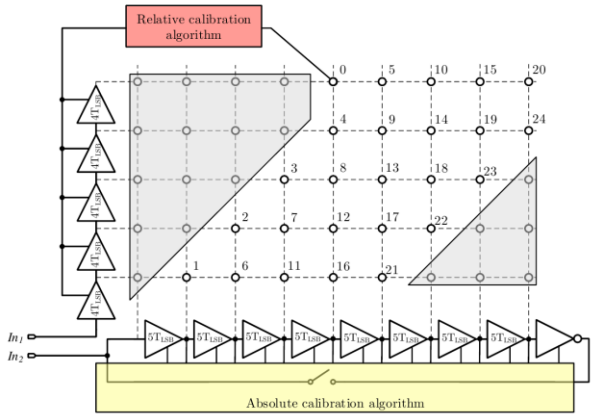
Background

Modern communication standards place high demands on the frequency generation in integrated circuits, especially with regards to low power consumption, low area, low phase noise and spurious tones. All-Digital Phase-Locked-Loops (PLL) in contrast to classical analog PLLs have an advantage in scaling better with advances to smaller CMOS nodes in terms of power and area consumption. However, designing such PLLs becomes more challenging especially for the low phase noise requirements and high suppression of in-band spurs.



Task

Therefore the aim of this thesis is the development of a control loop for AD-PLLs suitable for implementation in a 28nm technology.
Starting from schematics for the DCO and TDC their performance parameters need to be extracted and integrated into behavioral models. These models are then used to design the control loop in a hardware description language. State-of-art architectures should be investigated with regards to their performance in the targeted PLL system. The designed system is then to be synthesized to estimate the overall circuit performance, power and area consumption.



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