Design and Analysis of an Integrated Low Drop-out Regulator for All-Digital PLLs in 28nm Technology

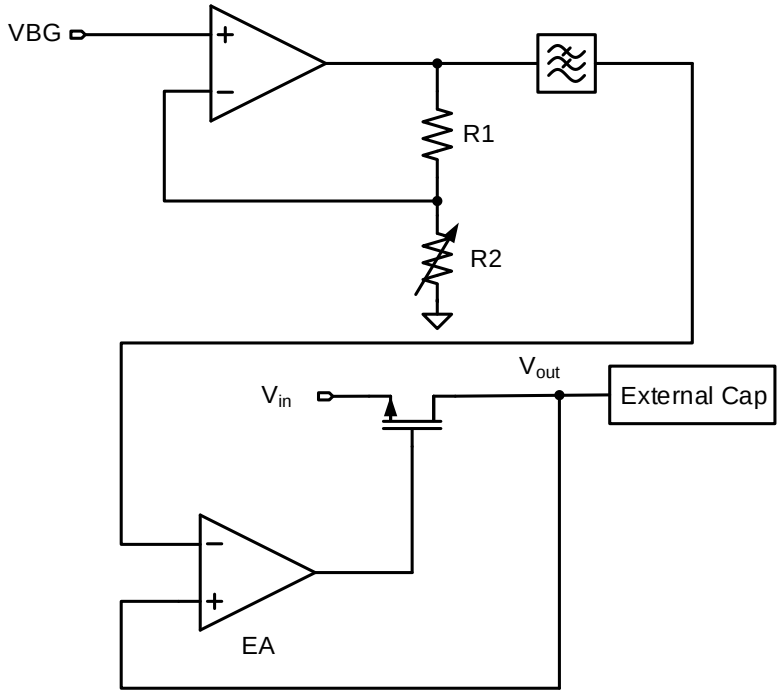
Background

All-digital phase-locked loop (ADPLL) has recently received intensive attention due to its good scalability, low power and area consumption. However, designing such PLLs becomes more challenging with increasing integration density and shrinking technology nodes. For example, fluctuation supply voltage can potentially influence output frequency directly and thus worsen the output phase noise. Hence, it is critical to have a stable supply voltage to satisfy high demanded specifications.

A low drop-out regulators (LDO) are critical components in the All-Digital PLL design since it provides a non-fluctuating voltage supply which has a direct impact on the AD-PLL performance. Thus, the goal of this thesis is to develop a low drop-out regulator in a 28nm technology that can meet the demand of an all-digital PLL application.

Task

Starting from the specification of the supply voltage sensitive blocks of the AD-PLL, performance specification of the LDO need to be determined. State-of-art circuitries should be investigated and comparison should be made in terms of their achievable performance. Afterwards, a suitable circuitry is to be implemented in 28nm technology and its performance is to be verified via simulation.



Contact / Supervisor

Lantao Wang

Kopernikusstr. 16, 52074 Aachen

ICT Cubes 2nd floor, Room 237

☎ 0241 80-20155

✉ lantao.wang@ias.rwth-aachen.de

Bachelor thesis – Marc Faßbender