Automated Parameter Extraction and Model Generation for Analog-to-Digital Converters

Background:

With the ever-increasing complexity in the design of analog-mixed signal circuits verification becomes an ever more challenging task. Verifying the proper functionality of top-level blocks such as an integrated Analog-to-Digital Converter (ADC) is a time and resource-consuming matter. Powerful tools that simplify and automate this task do not yet exist.

A novel tool tackling this challenge is currently developed at the chair of integrated analog circuits. By drastically reducing the complexity of the circuit down to an abstract mathematical model, a fast and efficient verification becomes possible. The required crucial parameters for the mathematical model are determined in a fully automated fashion beforehand, thereby further simplifying the entire verification process.

Task:

Taking a complex, continuous-time Sigma Delta (ΣΔ) Analog-to-Digital Converter as a reasonably complex use case, an automated parameter extraction and model generation tool shall be implemented. The implementation shall utilize the native programming languages of the Cadence Virtuoso Framework, a state-of-the-art analog-mixed signal circuit simulation program. In a first step an automated simulation flow has to be developed enabling the automatic extraction of important circuit parameters. Afterwards, these circuits parameters shall be utilized to generate an accurate model of the ΣΔ-ADC.

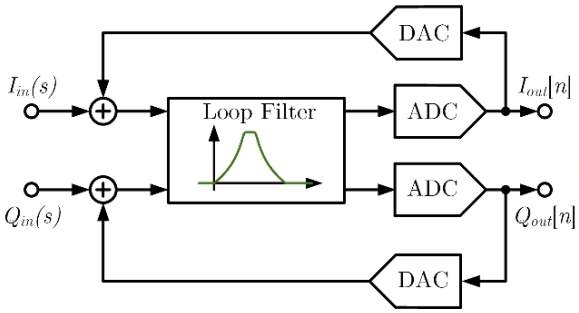

Fig. 1: Block Diagram ΣΔ ADC.

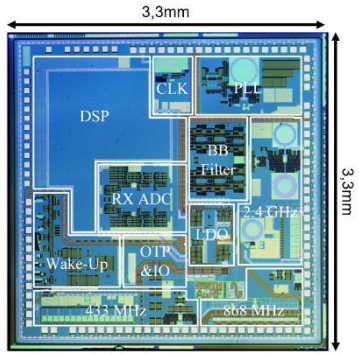

Fig. 2: Die photo ΣΔ ADC (RX ADC).

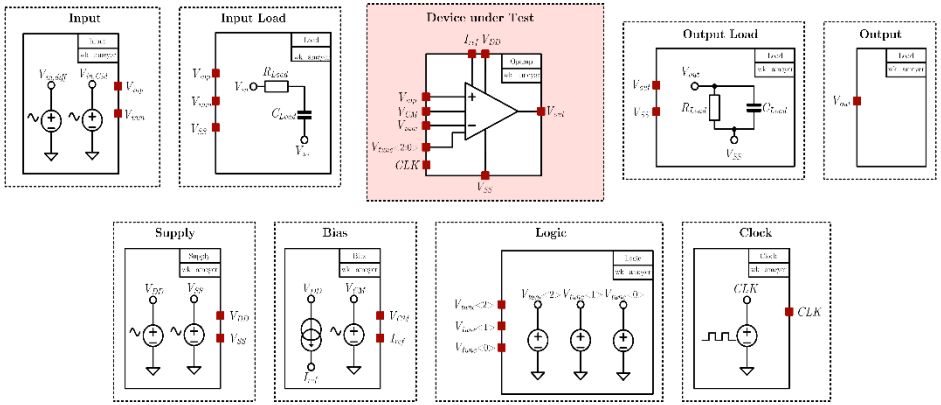

Fig. 3: Automated Testbench Generation.

Contact:
Alexander Meyer
☎ 0241 80-27749
✉ alexander.meyer@ias.rwth-aachen.de

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