Design and Implementation of a Time-to-Digital Converter for digital Silicon Photomultipliers

Background:

High energy physics (HEP) and preclinical positron emission tomography (PET) require a very accurate measurement of time of flight (TOF) for a precise reconstruction of flight paths or image reconstruction. Recent advancements in this field are focusing on the usage of Silicon Photomultipliers (SiPM) for a detection of single photon events and an accurate determination of TOF. A SiPM consists of multiple photodiodes exploiting the avalanche breakdown effect present in reverse-biased silicon pn-junctions. With high-energy photons hitting the SiPM's surface the avalanche breakdown can be triggered creating a signal which can be detected with Time-to-Digital Converters (TDCs). TDCs do not perform a typical analog-to-digital conversion in comparison to many other sensors, rather they directly convert the timing information of the signal into digital code. Hence, precise timing measurements can directly be made. As typically many SiPMs and TDCs are placed onto a single chip, a compact, highly efficient and scalable TDC design is desired.

Task:

This work aims at the design and implementation of a TDC for digital Silicon Photomultipliers with special emphasis on low power and area consumption. In a first step a suitable TDC architecture shall be identified. Afterwards, utilizing Cadence Virtuoso Framework, a state-of-the-art analog-mixed signal circuit simulation program, this architecture shall be implemented. During the design process, the robustness to process, temperature and supply variations has to be considered and compensated. Furthermore, as many TDCs are to be placed in close proximity, the mutual disturbance between several TDCs has to be studied.

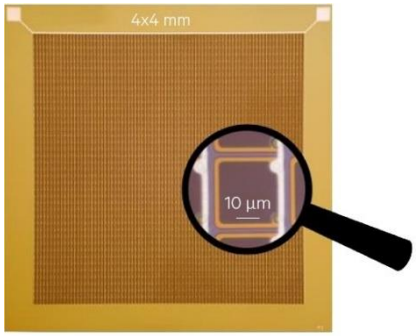

Fig. 1: Array of SiPMs

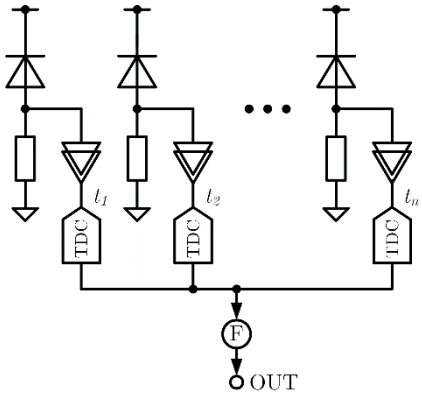

Fig. 2: Muti-channel dSiPM Concept

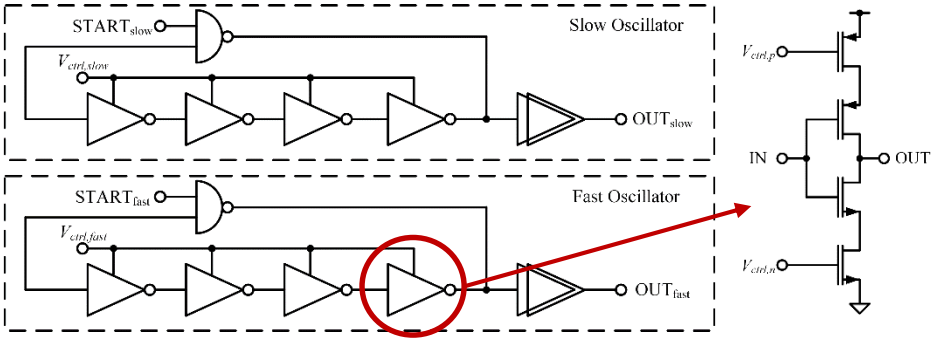

Fig. 3: Vernier Gated Ring Oscillator

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