Analysis of parasitic elements in high-speed DC-DC converters

Background
The power-electronic focused research at IAS is directed towards new applications and topologies of power-electronic circuits.

New semiconductor materials such as GaN or SiC have enabled the development of higher performance DC-DC converters, while significantly increasing the impact of parasitic circuit elements. Thus, the physical layout and packaging play an important role when switching in the megahertz-range.

While detailed EM simulations of RF-circuits are commonly employed, this type of simulation in power-electronics is still rarely used.

Analyzing and understanding the benefits and limitations of PCB-level EM-simulations in power-electronic applications is becoming more and more relevant due to increasing semiconductor performance and demands in switching converter performance.

Task
The proposed work aims to analyze the effects of parasitic elements in the operation of high-speed DC-DC converters through simulation and comparison by measurement of different powerstage designs.

The thesis can be written in English or German.

Bachelorthesis / Masterthesis

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